TIFR Centre for Interdisciplinary Sciences
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Seminar

Atomically Thin Chemical Switch – Gate Tunable Memristors based on Single Layer MoS_2

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Continued progress in high-speed computing depends on breakthroughs in both materials synthesis and device architectures. The performance of logic and memory can be significantly enhanced by introducing a memristor - a two-terminal device with internal resistance that depends on the history of external bias voltage. Memristor is a fundamental element in electrical circuits; however, its potential in commercial logic and memory circuits is just beginning to be realized. State-of-the-art memristors, based on metal-insulator-metal structures with insulating oxides such as TiO_2, are limited by a lack of control over filament formation and external control of switching voltage. Here, we report a new class of three-terminal memristors based on grain boundaries in single layer MoS_2. These devices provide widely tunable functions by confining electron and anionic transport to one-dimensional grain boundaries, and show switching ratios up to ~103 with dynamic negative differential resistance. Furthermore, due to the atomically thin nature of MoS_2, a third gate terminal in a field-effect geometry offers unprecedented control over electroformed device characteristics.

Thus, I will first introduce charge transport mechanisms in high quality MoS_2 transistors based on mechanically exfoliated flakes. Then, I will describe how varying stoichiometry of MoS_2 grown by chemical vapor deposition (CVD) can influence charge transport and device performance. Bulk of the talk will be dedicated to novel memristors and logic applications enabled by controlled defects and grain boundaries in CVD-grown MoS_2.

Tuesday, Dec 9th 2014

11:30 AM (Tea/Coffee at 11:15 AM)

Seminar Hall, TCIS